ONE TIME EXIT SCHEME

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10EC751

Seventh Semester B.E. Degree Examination, April 2018
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Why signal sampling is required? Explain the sampling process. **(05 Marks)**

b. Define decimation and interpolation process. Explain them using block diagram with relevant equations. **(06 Marks)**

c. Explain the major features of programmable digital signal processors. **(09 Marks)**

2 a. Write the structure of 4 × 4 Braun multiplier and explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on speed of the multiplier. **(10 Marks)**

b. What is the role of a shifter in DPS? Explain the implementation of 4 – bit shift right barrel shifter with a diagram. **(06 Marks)**

c. Explain the register pointer updating algorithm for circular buffer addressing mode. **(04 Marks)**

3 a. Explain the indirect addressing mode of TMS320C54XX processor. Give the operand syntax and operation for the following : i) circular addressing mode ii) bit reversed addressing mode. **(10 Marks)**

b. List the architectural features of three fixed point DSPS. **(06 Marks)**

c. Show all the bits of processor mode status register and explain the function of the following bits : MP/$\overline{MC}$, OVLY, DROM. **(04 Marks)**

4 a. Show the pipeline operation of the following sequence of instructions and if the initial value of AR3 is 80H and the values stored in memory locations 80, 81, 82, are 1, 2 and 3.

```
LD    *AR3+, A
ADD   # 1000H, A
STL   A, *AR3+
```

(08 Marks)

b. Give the logical black diagram of timer circuit. Explain its operation. **(06 Marks)**

c. Differentiate between MAC and MACD instructions. **(06 Marks)**

PART – B

5 a. What values are represented by the 16 bit fixed point number N = 4000h in the Q_7 and Q_{15} notation? **(04 Marks)**

b. Explain with the help of a block diagram and mathematical equation, the implementation of a second order IIR filter. **(10 Marks)**

c. Explain with necessary block diagram, memory organization for implementing FIR filters of order N. **(06 Marks)**

6 a. Write the signal flow graph for 8-point FFT implementation. Explain butterfly and Bit reversed index generation. **(12 Marks)**

b. Why zero padding is done before computing the DFT? **(02 Marks)**

c. Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP. **(06 Marks)**

7 a. Design a data memory system with address range 000800h – 000FFFhh for TMS320C5416 processor. Use 2K × 8 SRAM memory chip. **(10 Marks)**

b. Draw the flow chart of the interrupt handling by the TMS320C54XX processor and explain. **(10 Marks)**

8 a. With a sketch explain the JPEG encoder and decoder. **(10 Marks)**

b. Draw the block diagram of PCM3002 CODEC and explain. **(10 Marks)**

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